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A NEW METHOD OF REDUCING PHASE NOISE IN GaAs FET OSCILLATORS

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ABSTRACT

This paper addresses the problem of 1/f FM noise reduction in GaAs MESFET oscillators from circuit design considerations. The near-carrier FM noise is described with the aid of an analytic model that includes in-band and upconversion expressions. Variations in these terms are investigated as a function of circuit impedance. In particular, the bias impedance is observed to significantly affect the FM noise of the oscillator, primarily through the upconversion process. Techniques for noise reduction and experimental results are presented.

INTRODUCTION

Low noise oscillators are required in most microwave systems. Especially important are oscillators fabricated from three terminal devices. Techniques for the design of suitable oscillators, however, are not well established due to the complexity of the oscillator nonlinearities. Factors affecting the oscillator noise near the carrier, which is dominated by FM components, and the oscillator noise far from the carrier, which contains equal FM and AM components, were originally presented by Kurokawa [1] for microwave oscillators. Recently, Debney and Joshi [2] have extended Kurokawa's theory to analytically include the upconversion of device 1/f noise.

This paper deals with the effects of circuit impedances on oscillator noise. A technique is presented for the design of FET oscillators with minimized noise characteristics. The direct current resistance presented to the FET gate affects the low frequency FET noise contributions and their upconversion gain. Thus, this resistance influences oscillator noise near the carrier. Away from the carrier, the impedance of the resonator and feedback network affects the high frequency FET noise source contributions to the output noise. Oscillator impedances must be optimized for low noise just as amplifier impedances are optimized for low noise.

The optimization of the low frequency resistance in a bipolar transistor base circuit is straightforward since a low resistance would short out 1/f noise predominately in the base current. Since the 1/f noise voltage in an FET gate cannot be open circuited, there is no similar solution for an FET.

Noise reduction in FETs can occur through the use of a low frequency resistance in the gate circuit. The low frequency resistance allows the gate rectification current to optimize the oscillator gate bias voltage. Also, the resistance allows upconversion cancellations to occur between the gate rectification and Gm nonlinearities.

The importance of low frequency circuit resistances are demonstrated with common drain GaAs FET oscillators operating at 5.6 and 7.4 GHz. Reductions of up to 14 db in the phase noise of these microstrip oscillators are shown for low frequency resistances up to 200 kΩ.

THEORY

A complete description of oscillator noise can often be obtained from simple upconversion models (such as is developed in [2]). However, existing upconversion models do not include gate rectification. Near the carrier, a general description of the ratio of single sideband phase noise power per hertz bandwidth to carrier power is:

$$\mathcal{L}(f)=V_o^2 h(V_{gs},V_{ds},I_d,I_g,R)\cdot\frac{8\Gamma KTf_c}{G_m V_o^2 f}\cdot\left(\frac{f_o}{2Qf}\right)^2\cdot(1+\alpha) \qquad (1)$$

where V_o = the magnitude of the device output voltage,
R = the low frequency gate circuit resistance,
Γ = a device parameter (~1.0),
f_c = the device 1/f noise corner frequency,
f_o = the oscillation frequency,

$$\alpha=\frac{\frac{\partial Z}{\partial f}\cdot\frac{\partial Z}{\partial A}}{\frac{\partial Z}{\partial f}\times\frac{\partial Z}{\partial A}},$$

and $Z=[R_T(f,A)\ X_T(f,A)]^t$. The four groups of parameters in equation (1) can be respectively related to an upconversion gain, a squared ratio of the device input noise voltage to output voltage, the resonator transfer function, and a rela-

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tionship between oscillator impedance variations. The expression of α as a dot product divided by a cross product shows that a noise minimum occurs when the oscillator impedance variations with respect to frequency and amplitude are orthogonal. This observation is a natural result of theories such as Kurokawa's, but is not present in purely linear models such as Leeson's [3].

Since the contributions of device noise sources are affected by circuit impedances, the direct current resistance between the device gate and ground as well as the impedance of the resonant circuit near the oscillation frequency must be considered in oscillator design if optimum performance is to be obtained. The direct current resistance will affect the 1/f noise upconversion ($1/f^3$ phase noise response), while the high frequency circuit impedances will affect the $1/f^2$ and flat noise responses (oscillator noise floor). A low noise resistor, bypassed at high frequencies, will affect the noise upconversion by allowing the gate rectification current to produce a reverse bias on the gate. The upconversion cancellation by competing distortion mechanisms also occurs because of this resistor. The latter has a high sensitivity and rarely achieves a deep null because of the phase shifts due to circuit reactances. It is notable that the addition of a resistor in the gate circuit increases the low frequency noise because of a 1/f component in the gate noise current [4]. Low noise oscillator methods are limited to device improvements [5] and circuit techniques for large ratios of output voltage to upconversion gain.

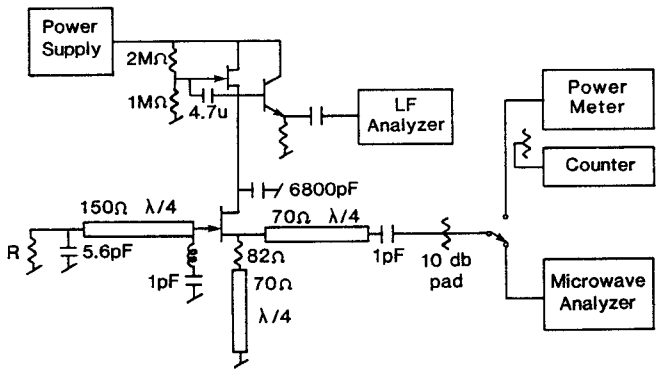

Fig. 1. Circuit used for examining effects of R on oscillator 1/f noise. The oscillator FET was an Avantek M106. The other devices were low frequency silicon transistors.

EXPERIMENT

To examine the effects of resistance in the gate-to-ground path at low frequencies, the circuit of Figure 1 was constructed. The microstrip circuit was etched on 31 mil thick 5870 duroid. The common drain oscillator used a packaged Avantek M106 GaAs FET with its frequency determined by a low Q series resonant circuit. The circuit between the power supply and the FET served as an active high pass filter. This filter allowed the low frequency FET noise to be observed when the FET was oscillating or quiescent. The low frequency gain of the FET through the active filter was measured so that the output noise could be referenced to the gate. Figures 2a and b show the measured low frequency noise of the quiescent FET. Note the 3 db per octave slope. The noise is enhanced by increases in bias and gate circuit resistance, as was shown in [4]. The noise increase with V_{gd} is correlated with the increasing gate leakage current. The noise increase with gate circuit resistance is due to a 1/f component in the gate noise current generator.

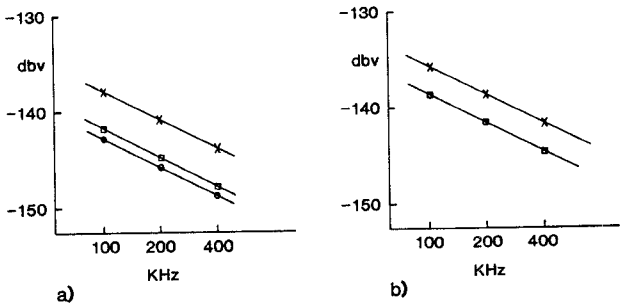

Fig. 2 a,b. Effective noise voltage of quiescent M106 GaAs FET as a function of bias and gate circuit resistance: (a) 2.7v V_d, 17.5 ma; (b) 5.7v V_d, 21 ma.

--x-- 200 kΩ R
--□-- 1 kΩ R
--o-- 0 Ω R

Figures 3 and 4 show £(f), the sideband noise power, for the 5.6 and 7.4 GHz oscillators as the gate circuit resistance was varied. The Qs of the oscillators were low enough so that a portion of the 1/f spectrum (note the 9 db per octave slope) could be observed directly on a spectrum analyzer. Note that the lowest noise was obtained when a gate resistance of 1 kΩ was used in the 5.6 GHz oscillator and 200 kΩ in the 7.4 GHz oscillator. The 14 db reduction in £(f) at 7.4 GHz represents an example of the degree to which the upconversion can be affected by the low frequency circuit resistances. While the output power was also affected by the low frequency circuit resistances, the reductions in noise surpassed the power loss.

Figure 5 shows experimental and calculated values of £(f) for various values of gate circuit low frequency resistance. The calculations used equation (1) with the common assumption that a given dc bias completely specifies the upconversion gain. The circuits were tuned for maximum power output with each gate resistance: 8.5 dbm with the 3.8 v/23 mA bias, and 5.9 dbm with the 3 v/18 mA bias. The difference between the measured and computed £(f) in Figure 5 is the reduction in upconversion gain caused by the gate circuit resistance. The fact that the £(f) shows a net increase with gate circuit resistance is due

to a reduction in oscillator Q caused by this resistor and an imperfect bypass at the 5.6 pF capacitor shown in Figure 1. Circuit layouts with improved bypassing are presently being designed.

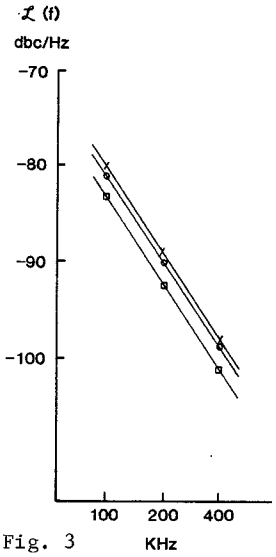

Fig. 3

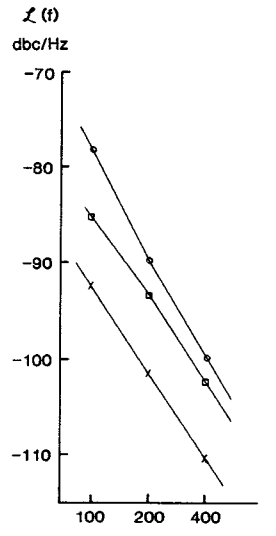

Fig. 4

Fig. 3. Phase noise of 5.6 GHz oscillator. The lowest noise was obtained with a 1 kΩ resistor in the gate circuit. The bias was 4.2v, 21 ma.

--x-- 200 kΩ R, P_o = 3.4 dbm
--□-- 1 kΩ R, P_o = 7.6 dbm
--o-- 0 Ω R, P_o = 8.8 dbm

Fig. 4. Phase noise of 7.4 GHz oscillator. The lowest noise was obtained with a 200 kΩ resistor in the gate circuit. The bias was 3.6v, 17.5 ma.

--x-- 200 kΩ R, P_o = -3.8 dbm
--□-- 1 kΩ R, P_o = -2.2 dbm
--o-- 0 Ω R, P_o = 1.2 dbm

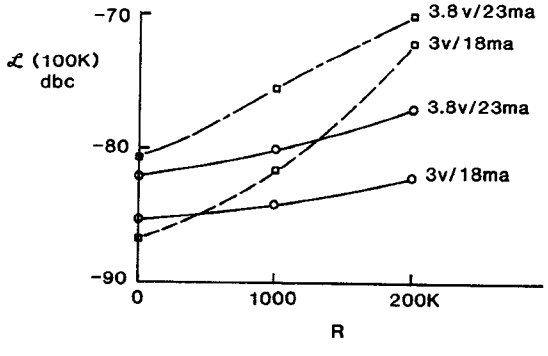

Fig. 5. ℒ(f) at 100 kHz for 5.6 GHz oscillation versus gate circuit resistance, R. The calculations assumed no change in upconversion for a fixed bias condition.
o---o measured
□---□ calculated (low bias)
□-·-□ calculated (high bias)

CONCLUSIONS

The oscillator circuit impedances at low frequencies have been shown to have large effects on the 1/f phase noise generated by an oscillator. The low frequency resistances change the phase noise by reducing the upconversion gain. The circuit impedances at high frequencies are known to affect oscillator noise outside the 1/f region. When these results are coupled it is possible to design oscillator circuits that provide optimized low noise performance.

REFERENCES

[1] K. Kurokawa, "Some Basic Characteristics of Broadband Negative Resistance Oscillator Circuits," Bell Sys. Tech. J., pp. 1937-1955, July-August 1969.

[2] B.T. Debney and J.S. Joshi, "A Theory of Noise in GaAs FET Microwave Oscillators and Its Experimental Verification," IEEE Trans. Electron Devices, vol. ED-30, no. 7, pp. 769-775, July 1983.

[3] D.B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum," Proc. IEEE, vol. 54, pp. 329-330, February 1966.

[4] M.D. Das and P.K. Gosh, "Gate Current Dependence of Low-Frequency Noise in GaAs MESFETs," IEEE Electron Device Letters, vol. EDL-2, no. 8, pp. 210-213, Aug. 1981.

[5] J. Graffeuil, K. Tantrarongroj, and J.F. Sautereau, "Low Frequency Noise Physical Analysis for the Improvement of the Spectral Purity of GaAs FET Oscillators," Solid-State Electron, vol. 25, no. 5, pp. 367-374, 1982.